

Fig. 1

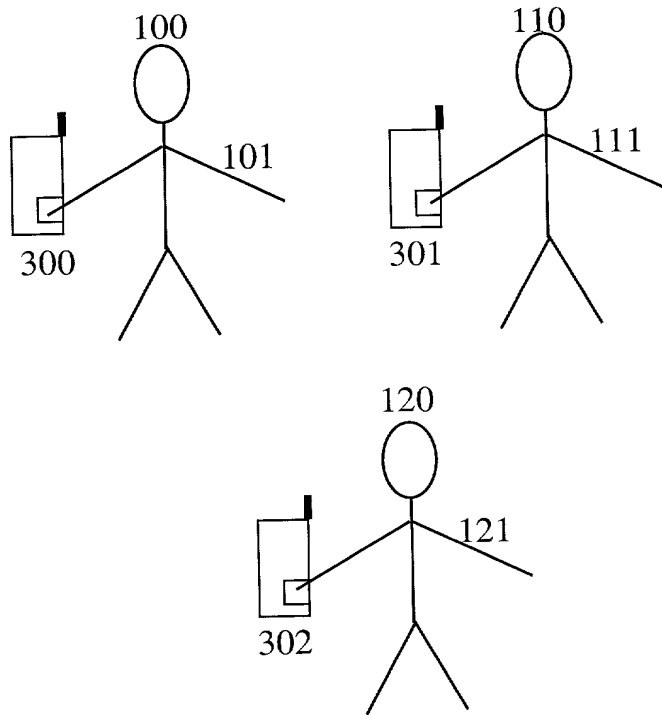
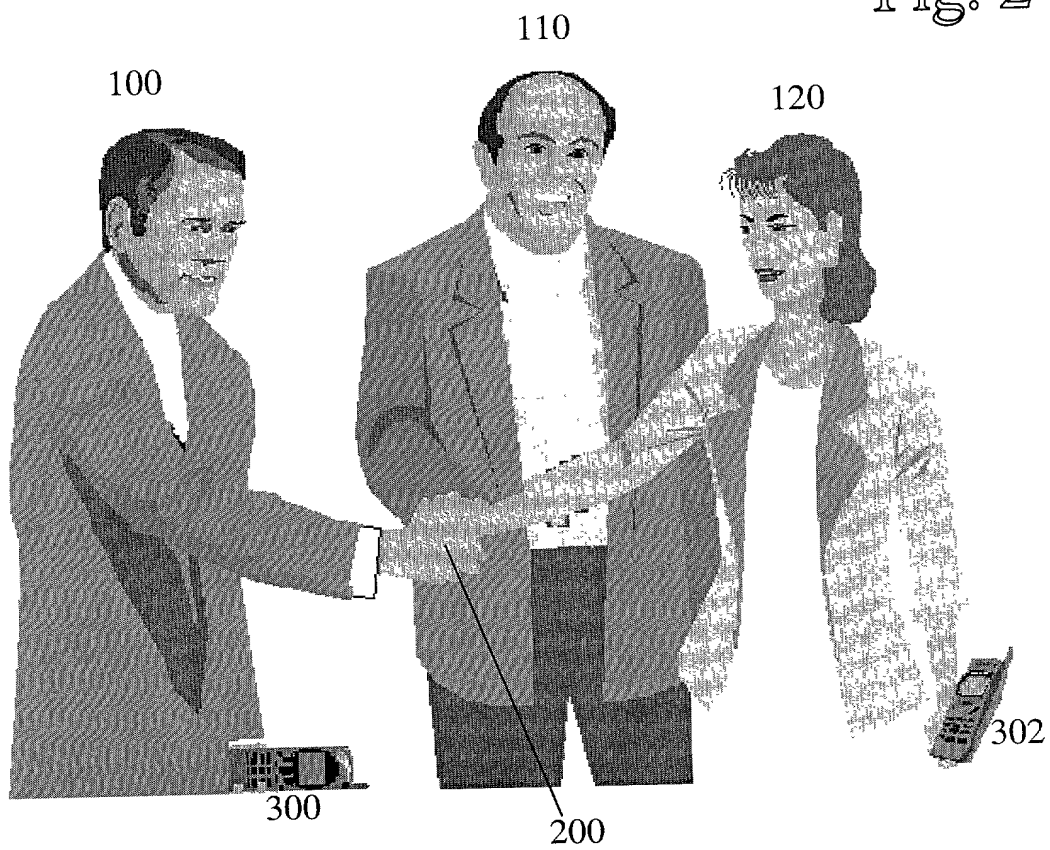


Fig. 2



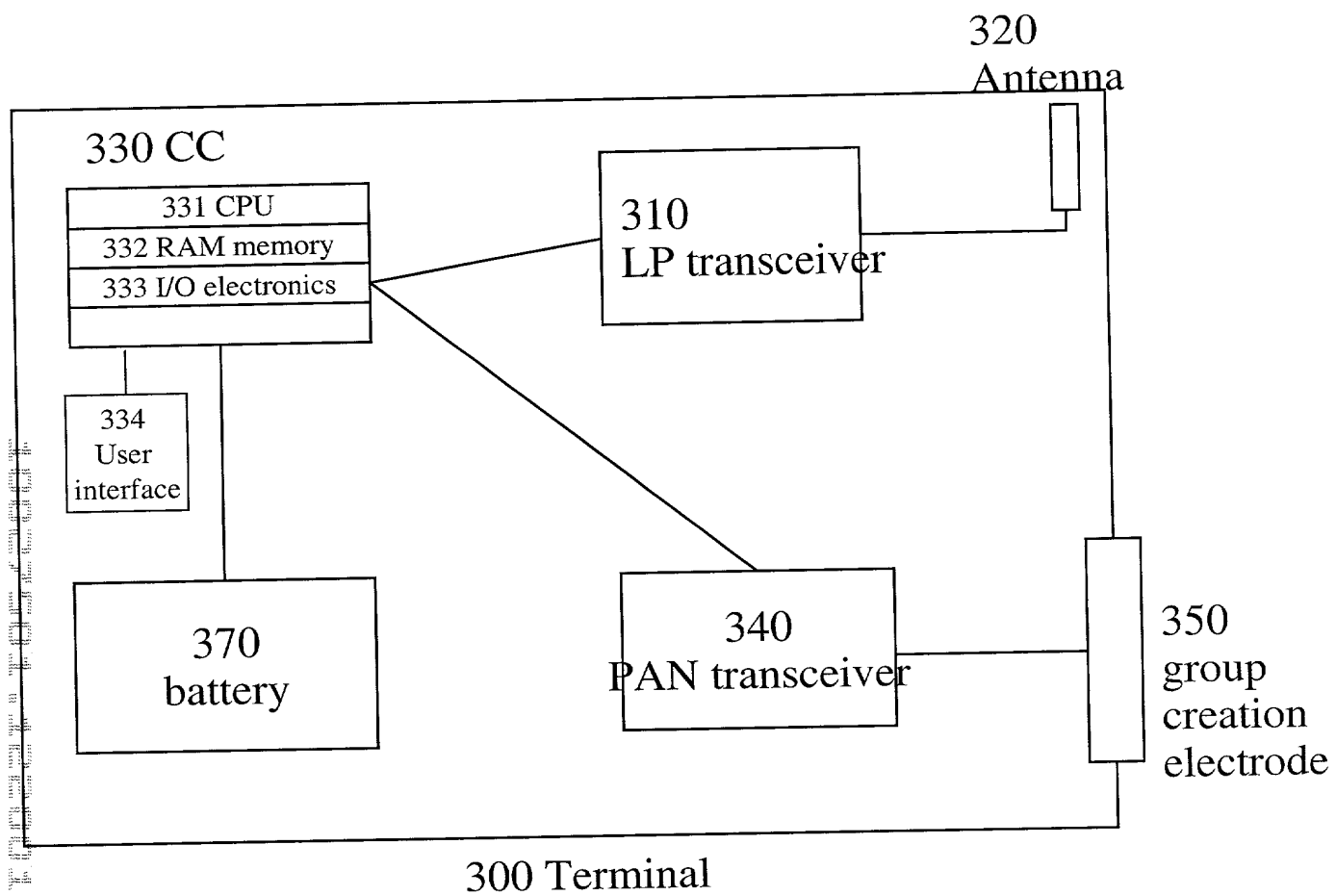


Fig. 3

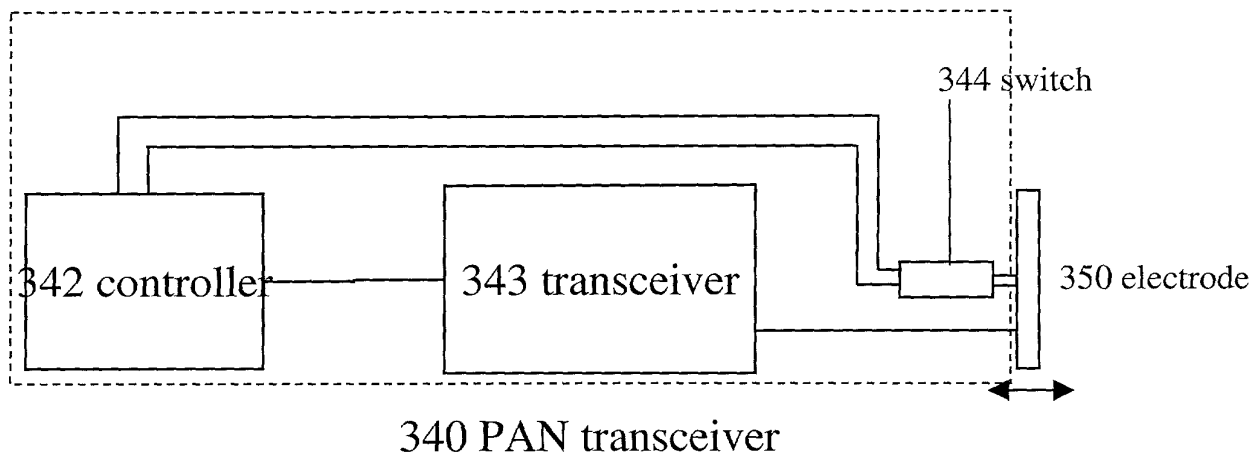


Fig. 4A

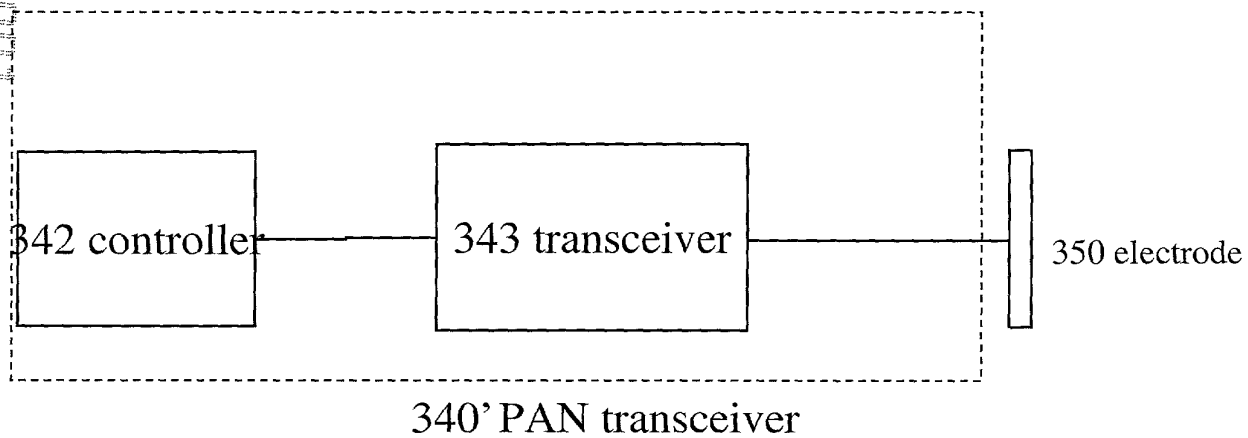
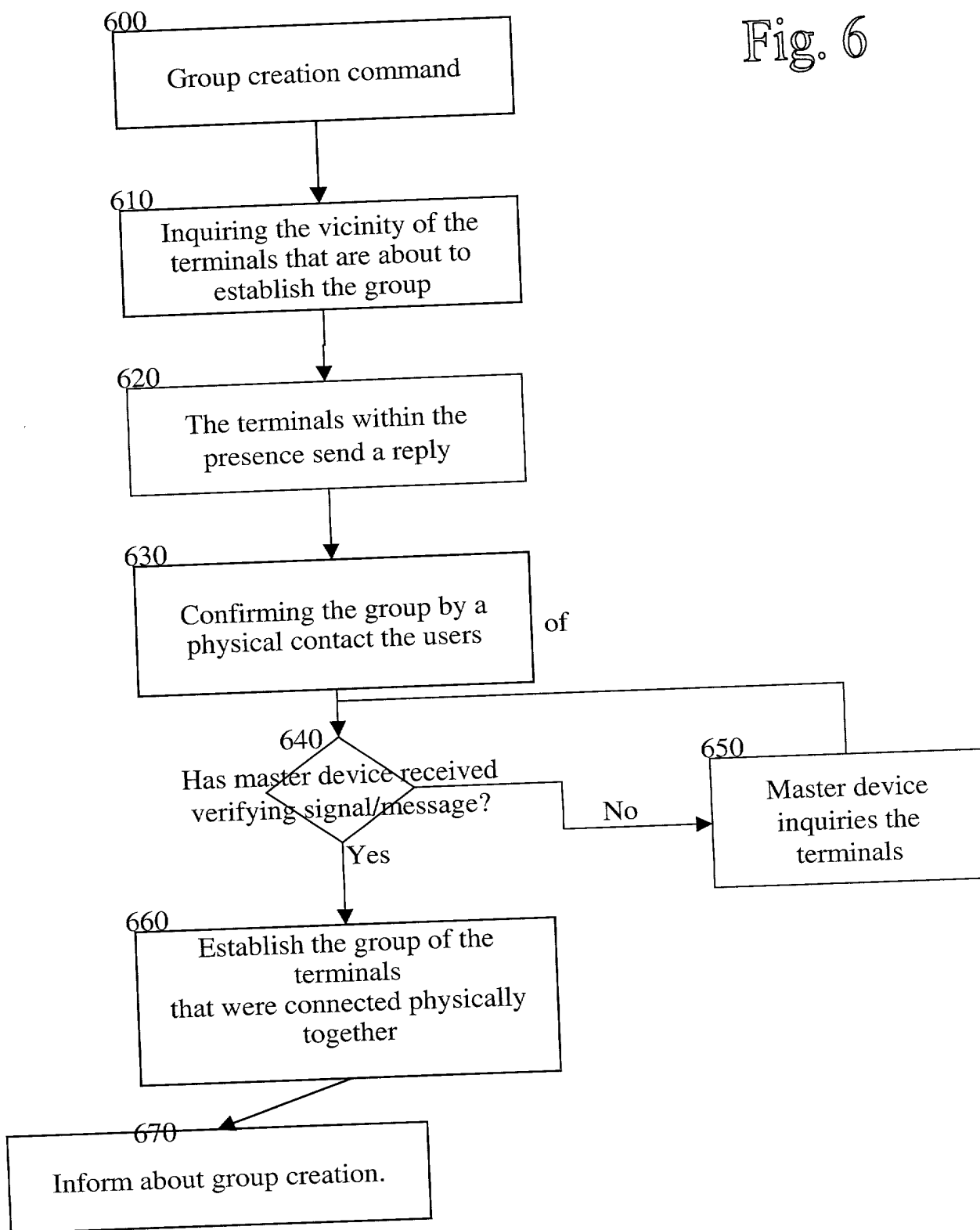


Fig. 4B

501	502	503
BD_ADDR	Clock Offset	Class of Device

Fig. 5

Fig. 6



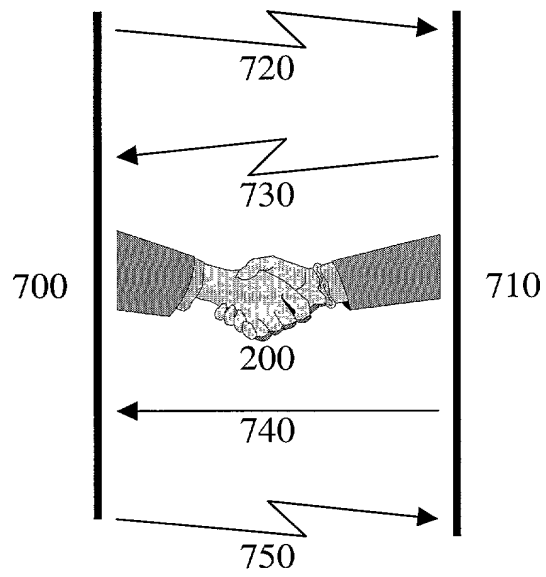


Fig. 7

Fig. 8

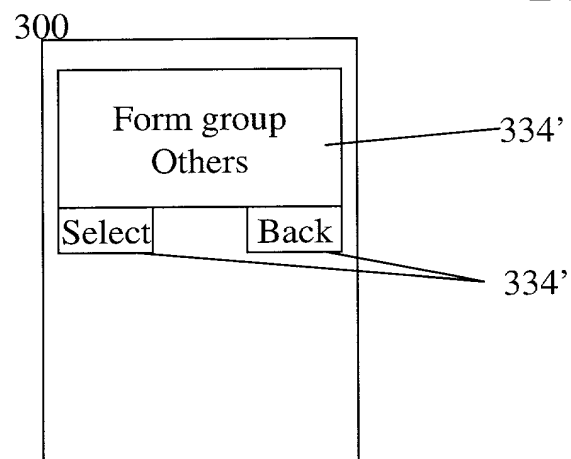


Fig. 9

